

Bare Die Semiconductor Performance

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Introduction

It can be difficult and expensive for designers of systems with limited area to determine how to accommodate changing functional requirements. Silicon packaging has evolved into a space-restraining process for many handheld, portable, and other tiny form-factor products. With that in mind, bare die availability has become a popular offering from Central Semiconductor. It offers the system or module designer the chance to make better use of the restricted area when compared to traditional semiconductor packaging.

Some applications of using a bare die in a system include application processors for mobile devices, image processors for digital still/video cameras and security cameras, and antennas for high-speed communication applications.



Benefits of using bare die

Due to the incorporation of die into circuit design, high-volume products like hearing aids, cell phones, and RFID cards are now more comfortable, and portable.

The advantages of using a bare die in embedded designs can be significant. Customers benefit from the availability of products in die form because it allows them to optimize their product designs for limited space and implement innovative, and proprietary module solutions.

There are additional advantages to using chips in system designs instead of packaged devices. Electronic circuits are contained in a smaller space, shortening the length of connections between chips, reducing the effects of capacitance and inductance, and minimizing switching delays. Electrical noise is also kept to a minimum. This is especially useful when high frequency signals are present in the system.

Designing a system with bare die

When designing a system with bare die you need to be consider how die performance changes once integrated into the system. Bond wire and lead frames will result in an increase in saturation voltages and impedance-based parameters. The material size and resistivity can be used to determine the added impedance, and with a test current value, can ultimately be converted to a voltage loss.

The lead frame plates, and bond wires increase parallel capacitance in the die process. This increases the semiconductor die's already existing junction capacitances. The junctions that the capacitance is contributing to in multi-terminal devices like FETs and BJTs must be carefully considered.

Added capacitance has a multiplicative effect on stored charge for end item parametric estimates. Calculating the time constants of additional capacitance, inductance, and resistance has an impact on switching speed. Modeling an equivalent resistance enables the calculation of this parameter.

Both construction and materials should prioritize signal transmission properties while minimizing parasitic elements that can adversely affect the signal. This includes selecting the proper length, diameter, and loop height of bond wire, along with the necessary thickness of lead frame and trace material to optimize current conduction. It is an ever-changing system, where additional compensation for one parameter can adversely affect another.

The lower inductance and capacitance of bare die integration is important in analog, RF, and power applications. Wire bonds and solder bumped die with shorter lengths have lower parasitic inductance than full packaged solutions. Improved full-system off-on times can be achieved by reducing cumulative capacitance in modules.



Conclusion

Bare die implementation offers higher degrees of integration, better signal integrity, and superior electrical performance while reducing weight and height. Designers can overcome the difficulties of small form factor applications by taking advantage of these features. Due to application performance requirements as well as physical system requirements, the implementation and rate of die products is rapidly rising, and Central Semiconductor is here to accommodate that need.

